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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,594	11/29/2001	Takashi Yamada	216692US2	2712

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/995,594	Applicant(s) YAMADA ET AL.
	Examiner Thomas L Dickey	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *16-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13 and 15* is/are rejected.

7)☒ Claim(s) *5 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The preliminary amendment filed on 07/06/98 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 1-15 in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Oath/Declaration

3. The oath/declaration filed on 22 March 2002 is acceptable.

Drawings

4. The formal drawings filed on 29 November 2001 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statements filed on 22 February 2002 and 14 June 2002 have been considered.

Specification

7. The title of the invention is not descriptive. A new title such as "SEMICONDUCTOR CHIP WHICH COMBINES BULK AND SOI REGIONS AND SEPARATES SAME WITH THREE ISOLATION REGIONS" is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 7-9 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the first, second and third insulators" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites the limitation " the third insulator" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation " the buried oxide " in line 2. There is insufficient antecedent basis for this limitation in the claim. For examination purposes it will be assumed that " the buried oxide " refers back the " a buried insulator" in claim 1 line 6.

Correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,2, and 10-13 are rejected under 35 U.S.C. 102(a) as being anticipated by LEOBANDUNG et al. (6,180,486).

With regard to claims 1 and 2, Leobandung et al. discloses a semiconductor chip a base substrate 10; a bulk device region 38 having a bulk growth layer 34 on a part of the base substrate 10, the bulk device region 38 having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer 34; an SOI device region 40 having a buried insulator 12 on the other part of the base substrate 10 and an SOI layer 14 on the buried insulator 12, the SOI device region 40 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer 14, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer, being the portion of bulk layer 34 that is located on the boundary,

located at the boundary between the bulk device region 38 and the SOI device region 40, wherein the bulk growth layer 34 is a silicon bulk growth layer, and the boundary layer reaches the base substrate 10 and is made of one of polysilicon or silicon-based compound semiconductors. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

With further regard to claim13, Leobandung et al. further discloses a dummy pattern 28 in the bulk device region 38 near the boundary. Note figure 7 of Leobandung et al.

With regard to claim 10, Leobandung et al. discloses a semiconductor chip comprising a base substrate 10; a bulk device region 38 having a bulk growth layer 34 on a part of the base substrate 10, the bulk device region 38 having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer 34; an SOI device region 40 having a buried insulator 12 on the other part of the base substrate 10 and an SOI layer 14 on the buried insulator 12, the SOI device region 40 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer 14, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer located at the boundary between the bulk device region 38 and the SOI device region 40, further comprising a first isolation 28 in the bulk device region 38, a second isolation 30 in the SOI device region 40, and a third isolation 32 positioned at the boundary and functioning as the boundary layer, the second isolation 30 being shallower than the third isolation 32. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

With regard to claims 11 and 12, Leobandung et al. discloses a semiconductor chip comprising a base substrate 10; a bulk device region 38 having a bulk growth layer 34 on a part of the base substrate 10, the bulk device region 38 having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer 34; an SOI device region 40 having a buried insulator 12 on the other part of the base substrate 10 and an SOI layer 14 on the buried insulator 12, the SOI device region 40 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer 14, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer located at the boundary between the bulk device region 38 and the SOI device region 40, and further comprising a first isolation 28 in the bulk device region 38, and a second isolation 32 that is shallower than the first isolation 28, the boundary layer being the second isolation 32 because the second isolation 32 is positioned closest to the boundary, wherein the second isolation 32 functions as the boundary layer, and has a bottom face that is in contact with the "buried oxide" 12. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

Claims 1,3,4, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by CHEN et al. (6,214,653).

With regard to claims 1,3, and 4, Chen et al. discloses a semiconductor chip with a base substrate 101; a bulk device region (labeled "High power circuits for CMOS DRAM/BULK") having a bulk growth layer on a part of the base substrate 101, the bulk

device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer; an SOI device region (labeled "logic, high speed circuits for CMOS/SOI) having a buried insulator 102 on the other part of the base substrate 101 and an SOI layer (marked "Si") on the buried insulator 102, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer 104 (left most instance) located at the boundary between the bulk device region and the SOI device region, wherein the bulk device region includes a first isolation 104 (left most instance) separating the bulk device, and the SOI device region includes a second isolation 104 (middle instance) separating the SOI device, the first and second isolations being of substantially the same depth and the first and second isolations have a depth reaching the buried insulator 102. Note figure 1D of Chen et al.

With regard to claim 6, Chen et al. discloses a semiconductor chip with a base substrate 101; a bulk device region (labeled "High power circuits for CMOS DRAM/BULK") having a bulk growth layer on a part of the base substrate 101, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer; an SOI device region (labeled "logic, high speed circuits for CMOS/SOI) having a buried insulator 102 on the other part of the base substrate 101 and an SOI layer (marked "Si") on the buried insulator 102, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the

first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer 104 (left most instance) located at the boundary between the bulk device region and the SOI device region, further comprising a first isolation 104 (right most instance) in the bulk device region, a second isolation 104 (middle instance) in the SOI device region, and a third isolation 104 (left most instance) positioned at the boundary arid functioning as the boundary layer, the first, second, and third isolations being of substantially the same depth. Note figure 1D of Chen et al.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over LEOBANDUNG ET AL. (6,180,486) in view of SATO et al., 2000 symposium on VLSI Technology Digest, pages 82-83 (13 June 2000).

Leobandung et al. discloses a semiconductor chip with all the limitations of claim 15 except a DRAM cell in the bulk region having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of

the first part being greater than that of the second part. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

However, Sato et al. discloses a DRAM cell in a bulk region having a trench capacitor (identified as the combination of the "storage node" and the "storage node plug"), the trench capacitor comprising a first part ("storage node") extending at and below the interface between the base substrate and the bulk growth layer, and a second part ("storage node plug") extending above the interface, the width of the first part being greater than that of the second part. Note figure 2 of Sato et al. Therefore, it would have been obvious to a person having skill in the art to augment Leobandung et al.'s semiconductor chip with the DRAM cell in a bulk region having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part, such as taught by Sato et al. in order to compactly combine logic circuits and memory circuits on a single chip.

Allowable Subject Matter

11. Claims 7-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112 set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. Claims 5 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
03/2003